Advances in Low-Defect Multilayers for EUVL Mask Blanks

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Advances in low-defect multilayers for EUVL mask blanks

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ABSTRACT

Low-defect multilayer coatings are required to fabricate mask blanks for Extreme Ultraviolet Lithography (EUVL). The mask blanks consist of high reflectance EUV multilayers on low thermal expansion substrates. A defect density of 0.0025 printable defects/cm² for both the mask substrate and the multilayer is required to provide a mask blank yield of 60%. Current low defect multilayer coating technology allows repeated coating-added defect levels of 0.05/cm² for defects greater than 90 nm polystyrene latex sphere (PSL) equivalent size for lots of 20 substrates. Extended clean operation of the coating system at levels below 0.08/cm² for 3 months of operation has also been achieved. Two substrates with zero added defects in the quality area have been fabricated, providing an existence proof that ultra low defect coatings are possible.

Increasing the ion source-to-target distance from 410 to 560 mm to reduce undesired coating of the ion source caused the defect density to increase to $0.2/\text{cm}^2$. Deposition and etching diagnostic witness substrates and deposition pinhole cameras showed a much higher level of ion beam spillover (ions missing the sputter target) than expected. Future work will quantify beam spillover, and test designs to reduce spillover, if it is confirmed to be the cause of the increased defect level. The LDD system will also be upgraded to allow clean coating of standard format mask substrates. The upgrade will confirm that the low defect process developed on Si wafers is compatible with the standard mask format 152 mm square substrates, and will provide a clean supply of EUVL mask blanks needed to support development of EUVL mask patterning processes and clean mask handling technologies.

Keywords: Extreme Ultraviolet Lithography, EUVL, Next Generation Lithography, NGL, mask, multilayer, defect, defect detection, defect mitigation.

1. INTRODUCTION

Extreme Ultraviolet Lithography (EUVL) is the leading Next Generation Lithography (NGL) technology to succeed optical lithography beyond the 70nm critical-dimension node. EUVL uses a wavelength of 13.4nm, and is under development by a partnership of three DOE national laboratories and industrial sponsors. The Engineering Test Stand (ETS) is an alpha-class exposure tool built to demonstrate full-field (106 X 132 mm on mask) printing at 4X reduction at the 100nm node. It includes full environmental controls and a 10 wafer per hour throughput for 200 mm wafers. The ETS has successfully printed 70nm features across its full field. A more complete technical description of EUV Lithography can be found in the 1999 EUVL White Paper.

To achieve imaging at 13.4nm, EUVL uses all reflective optics. The optical surfaces are coated with thin multilayer coatings to provide approximately 70% reflectance.⁴ The multilayers comprise 81 alternating Mo and Si layers with a 6.9nm period, for a total multilayer stack thickness of about 280nm. Spiller⁵ has published an extensive treatment

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of EUV multilayer coatings and a further description of the EUVL mask architecture is presented in the EUVL White Paper.

In order to provide mask blanks (defined as the multilayer-coated mask substrate) at reasonable cost and yield, the multilayer deposition process must be nearly defect free, and have uniformly high EUV reflectance, low stress and uniform thickness. The substrate must be of low thermal expansion material with stringent flatness, roughness and defect requirements. The full set of requirements for the EUVL mask has been described by Hector et al.⁶

A low defect density (LDD) multilayer deposition tool has been developed to provide low defect coatings for EUVL masks. ^{7,8,9} The system uses argon ion beam sputter deposition, and is equipped with full SMIF (standard mechanical interface) handling of 200 mm silicon wafers to minimize the number of defects added by handling. Silicon wafers were chosen as the substrate for defect reduction for the following reasons:

- defect inspection tools for unpatterned wafers are available at reasonable cost which have high sensitivity (75-90 nm PSL equivalent on multilayers) and fast speed (2 min per wafer). Equivalent tools for standard format masks do not exist, or have only recently come to market.
- ultra clean wafers are available with defect density before coating of 0.05 defects/cm²; these wafers are four times less expensive than fused silica mask substrates.
- low defect, robotic SMIF handling equipment for wafers is more advanced than for masks. Standard hardware can be purchased that allows automated processing of lots of 25 wafers with handling-added defect densities of only 0.008 defects/cm².

Defect reduction strategy

Two complementary strategies are being used to fabricate defect-free EUVL masks. The strategy is based on the observation that the multilayer deposition process, under certain processing conditions, smoothes small defects. ^{10,11} These tiny defects if not smoothed would become "printable" defects. They also represent a challenge to the current defect inspection infrastructure because there is no concept for an inspection tool with reasonable throughput and sensitivity for defects below 30nm. The strategy therefore is to: (1) develop low defect substrate polishing and multilayer deposition systems which add no defects larger than 50 nm; and (2) develop the multilayer deposition process so that it smoothes all defects smaller than 50 nm. There will probably still be a need for an inspection tool with around 30 nm sensitivity to capture defects that are near the cutoff at which smoothing is effective, or added in the middle of the deposition process.

Low defect coatings on standard square format mask blanks

The low defect deposition tool is being modified to coat standard square format mask blanks while retaining the capability to coat 200mm wafers. Figure 1 shows a plan view of the deposition system with the addition of the reticle SMIF pod (RSP) robotics. Coating system cleanliness will be verified on the wafer format, after which standard format blanks will be processed. The targeted defect density for the coatings is $0.1/\text{cm}^2$ for the first phase of the upgrade. The substrates will require backside conductive coating to allow use of the existing electrostatic chuck, which is cleaner than mechanical clamps that get coated and become a source of particulates. The reticle SMIF pod (RSP) standard based on the 200mm wafer SMIF standard will be used. It has the advantage that it securely grips the substrates by the bevels and is most compatible with maintaining blank cleanliness during shipping. Clean shipping is critical since the blanks will be shipped offsite for both the pre-coating and post-coating defect inspection.

Clean metrology systems to measure EUV reflectance are also important because it is required both before and after the mask patterning process to measure changes in the optical performance of the multilayer. The LDD upgrade will take advantage of the laser-plasma-based EUV reflectometer already integrated into the LDD, which has been shown to add less than 1 defect per substrate. This is in comparison to EUV metrology at synchrotron-based beam lines, which currently utilize manual handling of the masks and therefore add thousands of particles to the mask blanks. The upgrade is supported in part by International Sematech, with expected completion in summer 2002.

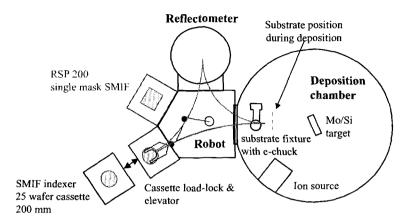


Figure 1. Plan view of the low defect deposition system with the addition of the reticle SMIF pod (RSP) robotics for coating standard format mask blanks.

2. DEFECT REDUCTION PROGRESS AND DEPOSITION SYSTEM IMPROVEMENTS

Low defect ion beam sputter deposition of multilayers requires careful attention to the following components:

- substrate robotic handling systems and cleanroom practices
- a low particulate ion source
- pure, low-inclusion molybdenum and silicon sputter targets
- clean deposition chamber shielding which resists flaking and particulation even after extended operation and buildup of thick deposition.

Our progress in defect reduction through January 2002 is shown in Figure 2. The figure shows all defects above 90nm size (measured by latex sphere equivalent scatter size), which is our current limit of reliable detection on multilayer-coated blanks. Much of the fluctuation in the figure results from specific experiments aimed at modifying the deposition tool and process rather than from lack of process stability. While only modest gains have been made in the defect density achieved during the cleanest operation, we have made improvements in our ability to repeatedly achieve defect densities of around $0.05/\text{cm}^2$. Extended clean operation of the coating system at levels below $0.08/\text{cm}^2$ for 3 months of operation was also achieved in the spring of 2001. The interim milestone of adding 0.01 defects/cm² or fewer has been met on several blanks. To put the defect density in perspective, the right hand side of Figure 2 shows the number of added defects per 200mm wafer: a defect density of $0.1/\text{cm}^2$ corresponds to 25 defects per wafer, and $0.01/\text{cm}^2$ corresponds to only 2.5 added defects. Table 1 lists the number of added defects per 200 mm wafer for a variety of defect densities. It also lists the number of added defects that would appear in the quality area of an 88 X 132 mm mask. A defect level of $0.003/\text{cm}^2$ has been estimated to be required to achieve a 60% yield on the manufacturing of defect free mask blanks. The properties of the properties

Table 1. Number of added defects per substrate for wafers and masks at a variety of defect densities

Defect density*	Added defects per substrate		Comment
(defects/cm ²)	200 mm wafer	mask (88 X 132 mm)	
0.1	25	12	
0.05	13	6	current repeatable level
0.01	2.5	1.2	
0.003	0.75	0.3	required for 60% yield

^{*} at current inspection sensitivity of 90 nm PSL sphere equivalent size

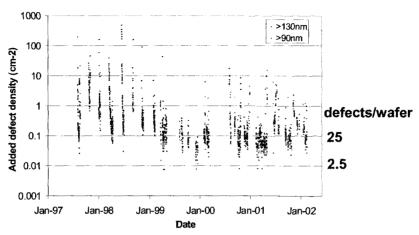


Figure 2. Progress in defect reduction through 2002. Each data point represents a single substrate.

We have fabricated 2 multilayer-coated wafers in which all of the added defects were outside the 88 X 132 mm quality area of a mask. Figure 3 shows the defect maps for those 2 wafers. The defects are typically distributed uniformly across the wafers—the fact that the added defects all appeared near the edge for these 2 substrates appears simply to be a case of favorable statistics.

Figure 2 suggests that an accelerated learning rate is required to achieve the required defect density in time for commercialization of EUV lithography. To that end, we have developed an improved set of deposition shielding to allow faster turnaround on chamber modifications than our previous shielding. The shielding is used to protect the permanent chamber hardware from getting coated with molybdenum and silicon during deposition; the coating buildup would subsequently flake and increase defect levels. The advantage of removable shielding is that it is more easily cleaned and allows use of a wider variety of materials and surface treatments to optimize performance and longevity before cleaning is required. Figure 4 shows photographs of the new shields installed in the coating chamber. The new shields are composed of heavy gauge stainless steel that has been alumina grit blasted to remove coatings and provide a textured, flake resistant surface. A commercial supplier performs the grit blasting and subsequent cleaning of the shields. Although the new shields have been designed for rapid removal and installation, their primary advantage lies in the fact that we can now vent the chamber, modify the hardware, evacuate the system, and resume deposition cleaner than 0.1defects/cm². This is in contrast to shields used in the past, which would flake after a single exposure to atmosphere after coating. The requirement of a full chamber maintenance after every chamber vent greatly slowed progress because of the large size (2m diameter) of the LDD chamber and the complexity of the chamber components.

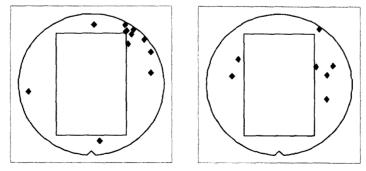
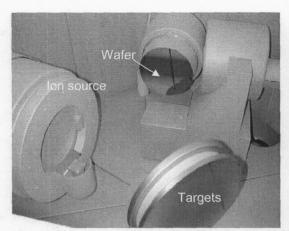


Figure 3. Defect maps for 2 multilayer coated wafers in which all of the added defects were outside the 88 X 132 mm quality area of a mask.



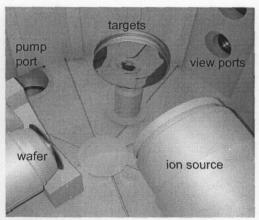


Figure 4. Photographs of the new deposition chamber shielding used to allow faster turnaround on chamber modifications.

The new shield set enabled multiple sets of experiments in which the ion source was moved to increase the distance between the ion source and the target from 410 to 560 mm. The primary advantage of the increased distance is reduction in coating of the internal surfaces of the ion source with Mo and Si. Flaking, particle formation, and erosion of ion source components associated with coating of the source with Mo and Si have been observed during maintenance of the source. We also see an increase in the RF power required to sustain the plasma in the source as the coating thickness builds up over time. A freshly maintained source requires a power of only 400 W to provide an ion beam current of 300 mA, compared to 1000W or more after hundreds of depositions. The coating on the bowl absorbs the additional RF power; this is dissipated as heat, which is certain to cause the ion source to undergo large temperature fluctuations between lots of wafers. These results are for the newer Veeco RIM-210 ion source design—the older design was even more sensitive to buildup of conductive coating. An additional advantage of the larger ion source-to-target distance is improved target utilization achieved by moving the target out of the focal point of the ion source. One of the risks of the increasing the distance is increased ion spillover, defined as argon ions that miss the target and strike other components in the chamber. The original design of the LDD used the large 300 mm targets to provide 0.1% or less spillover. Simulations of the ion beam by the Veeco source designers 14,15 were used to lead the decision on how far to move the source and provide assurance that there would not be a large degradation in spillover.

Figure 5 shows results of the experiments with the increased distance. The plot shows results of 6 runs, each run consisting of 20 or more depositions. It is clear from the data that the larger source distance increased the defect level by about a factor of 3. The primary advantage of the new shields is that it allowed confirmation that the effect shown in Figure 5 is repeatable and truly attributed to the change in ion source distance and not by some other effect, such as degradation of the cleanliness of the shields or ion source.

A set of deposition rate and ion beam spillover diagnostics was installed at various locations in the LDD tool to ascertain the cause of the increased defect level. Three types of diagnostics were used, and are shown in the photographs of Figure 6 for both source-to-target distances.

- 1) A 150 X 450mm copper plate was installed vertically at the chamber wall in the location where beam spillover missing the target was suspected to be highest. The copper surface has a high color contrast to the Mo and Si coating and allows much better visualization of deposition vs. etching as compared to the stainless steel shielding, for which the appearance does not provide a clear indication of etching and deposition rates.
- 2) Glass witness slides were used to monitor deposition and etching rates at various locations in the chamber. Strips of Kapton tape were used to mask regions of the slides to allow quantitative measurements of the rates. Qualitative results were obtained by observing the opacity of the films.
- 3) Glass witness slides were placed behind 6mm diameter apertures to measure directionality of deposition. These are termed "deposition pinhole cameras".

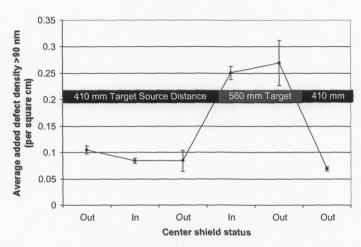


Figure 5. Defect data from multiple sets of experiments in which the distance between the ion source and the target was increased from 410 to 560 mm.

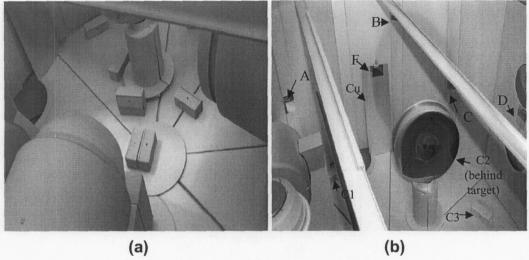


Figure 6. Photographs of the deposition chamber with the diagnostic witness plates and pinhole cameras. The ion source-to-target distance is 410 mm (original configuration) in Figure 6a and 560 mm in Figure 6b.

The diagnostics provided new understanding of deposition within the LDD. Beam spillover for the increased source-target distance was much larger than expected, as shown by the copper plate in Figure 6b. The dark area on the plate is a projection of where the circular target shadows the ion beam: net deposition occurs where the target blocks the beam; net etching caused by ion beam spillover occurs on the rest of the plate. This same behavior occurs for the original source-target distance as shown in Figure 6a, but to a lesser extent. The deposition witness slides provided quantitative measurement of the deposition and etching rates for both configurations. The locations of the witness slides are shown in Figure 7, and the measured rates are given in Table 2 for both configurations. Positive rates indicate deposition, negative rates indicate etching.

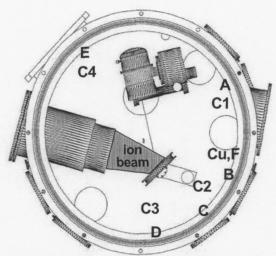


Figure 7. Plan view drawing of the deposition chamber with the locations of the deposition and etching rate diagnostics. Cu = copper plate, A-F = witness slides, C1-C4 = pinhole cameras

Table 2. Deposition and etching rates measured at various locations in the deposition tool

Witness Sample *	Thickness: (Å)		
	source to target = 41 cm	source to target = 56 cm	
A	5120	4550	
В	2310	-900	
С	2230	2400	
D	180	120	
E	28400	28600	
Cu, F	3430	1000	

^{*} Location numbers are referenced to Figure 7. Negative values indicate etching.

The deposition pinhole cameras gave valuable information about the source of the etching and deposition. Their locations are also shown in Figure 7. For every pinhole camera that had line of sight exposure to the ion source, there was an etched spot on the slide that projected back to the ion extraction grids. The etched spots indicate that the intensity of beam spillover is much higher than previously thought. The etched spots occurred even for pinhole cameras that were placed at angles of 30° from the axis of the ion beam, which is much higher than the 3.5° predicted divergence of the ion source. These "tails" of the ion beam may be a significant initiator of particle generation in the spillover regions even though they are orders of magnitude less intense than the primary beam. The most plausible explanation for the high spillover and divergence is that ion-neutral charge exchange collisions within the ion extraction gridset generate ions that are improperly accelerated as compared to ions that properly enter the gridset from within the plasma. The charge exchange ions see only part of the electric field designed for the gridset and can therefore be accelerated to angles and energies very different from those desired. The high level of spillover does not necessarily conflict with published measurements of the ion beam profile. In those studies the ion beam extraction model could only be validated in the core of the beam where the ion current is highest. The beam current in the tails is much lower and difficult to quantify experimentally. Nonetheless the current in the beam tails may play a significant role in particle generation.

The pinhole cameras also provided qualitative evidence that gas phase scatter of the deposition flux is relatively minor. There appeared to be 2 primary sources of deposition. As expected, most of the deposition was line-of-sight from the center of the target. The second source of deposition came from the direction of the substrate and the substrate fixture—deposited Mo and Si get re-etched by energetic neutral argon atoms reflected from the targets. This effect is particularly strong for the 30° target angle used that directs specularly reflected atoms to the substrate and fixture. The reflected neutral beam is also known to be more intense for the Mo target compared to Si because of the mismatch in atomic mass between Ar and Mo.

Figure 8 depicts a summary of our new understanding of the deposition and etching within the LDD. Three zones have been identified as depicted by the different shading:

Zone 1: Shields with line of sight to the target being sputtered have thick deposition as expected. We also know that the maximum flux from the target is in the direction of the specularly reflected beam for the 780eV Ar ions used in this study. Deposition rate falls off away from the specular direction.

Zone 2: Shields without line of sight to the target face, but with line of sight to the ion source are etched by spillover ions.

Zone 3: Shields without line of sight to the target or the source have thin deposition that mostly arrives from the wafer fixture. An example of this region is the area shadowed from the ion beam by the targets.

The copper plates and the witness slide data in Table 2 show that the larger source-target distance caused a large increase in beam spillover. It is possible that the increased spillover for the larger source-target distance was the primary cause of the increased defect level. Current efforts are underway to quantify beam spillover, then test designs to reduce it if it is confirmed to be the cause of the increased defect level.

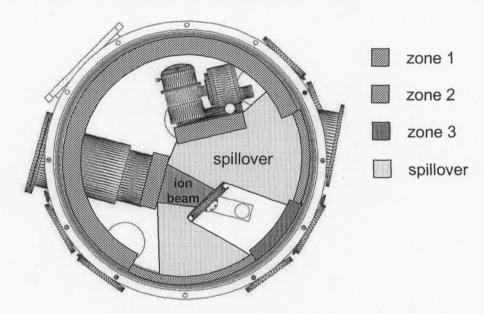


Figure 8. Locations of the 3 deposition and etching zones in the LDD. See text for descriptions of the zones.

5. CONCLUSIONS

We have continued to reduce the defect density of Mo/Si multilayers and can now repeatedly achieve a defect density of 0.05 defects/cm² at 90nm inspection sensitivity. Extended clean operation of the coating system at levels below 0.08/cm² for 3 months of operation has also been achieved. We have fabricated 2 coatings that were free of defects in the 88 X 132mm mask quality area. Increasing the ion source-to-target distance from 410 to 560 mm to reduce undesired coating of the ion source caused the defect density to increase to 0.2/cm². Deposition and etching diagnostic witness substrates and deposition pinhole cameras showed a much higher level of ion beam spillover (ions missing the sputter target) than expected, which was a possible cause of the increased defect level. Future work will quantify beam spillover. New designs will be tested to reduce beam spillover if it is confirmed to be the cause of the increased defect level. The LDD system will also be upgraded to allow clean coating of standard format mask substrates. The upgrade will confirm that the low defect process developed on Si wafers is compatible with the standard format substrates. The upgrade will also provide a clean supply of EUVL mask blanks needed to support development of EUVL mask patterning processes and clean mask handling technologies.

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